WHAT IS CLAIMED IS:

1. A multilayer interconnection substrate comprising:

an uppermost interconnection layer having a plurality of terminal pads formed at positions corresponding to a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said multilayer interconnection substrate;

a metal column formed on each of said terminal pads;

a resin film covering a side surface of said metal column; and

an insulating layer formed on said uppermost interconnection layer so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film.

2. The multilayer interconnection substrate as claimed in claim 1, wherein a height of said metal column is smaller than a thickness of said insulating layer.

3. An interconnection substrate comprising:

an insulating base having a plurality of penetration holes;

a plating metal filling each of said penetration holes;

a terminal pad formed on an end of each of said penetration holes so that said terminal pad is connected to said plating metal, said terminal pad located at a position corresponding to a respective one of a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said interconnection substrate;

a metal column formed on said terminal pad;

a resin film covering a side surface of said metal column; and

an insulating layer formed on a surface of said insulating base on the same side as said end of each of said penetration holes so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film.

4. A multilayer interconnection substrate manufacturing method comprising the steps of:

forming a plurality of terminal pads in an uppermost interconnection layer;

forming an insulating layer on said uppermost interconnection layer;

forming openings in said insulating layer, the openings located at positions corresponding to said terminal pads;

filling each of said openings with metal particles;

forming a metal column in each of said openings by heating said metal particles at a temperature which melts said metal particles; and

removing a part of said insulating layer

near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column.

5. The multilayer interconnection substrate manufacturing method as claimed in claim 4, wherein the step of filling includes a step of filling each of said openings with said metal particles up to a predetermined level in the middle of each of said openings.

6. A multilayer interconnection substrate manufacturing method comprising the steps of:

forming a plurality of terminal pads on an uppermost interconnection layer;

forming an insulating layer on said uppermost interconnection layer;

forming openings in said insulating layer, the openings located at positions corresponding to said terminal pads;

forming a conductive layer on surfaces of said insulating layer and inner surfaces of said openings;

forming a plating metal on said conductive layer by electrolytic plating by using said conductive layer as an electric supply layer so that said plating metal fills said openings;

forming a metal column in each of said

openings by removing other parts of said conductive layer and said plating metal than a part formed in each of said openings by one of etching and polishing so that said conductive layer and said plating metal together form said metal column; and

removing a part of said insulating layer near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column.

7. A multilayer interconnection substrate manufacturing method comprising the steps of:

forming a plurality of terminal pads in an uppermost interconnection layer;

forming a conductive layer on said terminal pads;

forming a plating resist on said conductive layer;

forming openings in said plating resist, the openings located at positions corresponding to said terminal pads, so as to expose a part of said conductive layer formed on each of said terminal pads at the bottom of each of said openings;

forming plating metals on said part of said conductive layer exposed at the bottom of each of said openings by electrolytic plating by using said conductive layer as an electric supply layer so that said plating metals form a metal column in each of said openings;

removing said plating resist so as to expose parts of said conductive layer other than a

part where said metal column is formed;

removing said exposed parts of said conductive layer other than said part where said metal column is formed by etching;

forming an insulating layer all over said uppermost interconnection layer, leaving an upper surface of said metal column uncovered; and

removing a part of said insulating layer near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column.

8. The multilayer interconnection substrate manufacturing method as claimed in claim 7,

wherein said conductive layer is composed of a metal containing copper, and said metal column is composed of solder, and

wherein the step of removing said exposed parts of said conductive layer is performed using an etching solution, an etching rate of said etching solution with respect to copper being higher than an etching rate of said etching solution with respect to solder.

9. An interconnection substrate manufacturing method comprising the steps of:

forming an insulating base having a plurality of penetration holes therein and a

conductive layer for terminal pads formed on one surface thereof;

forming a plating resist on said conductive layer for terminal pads;

forming openings in said plating resist, the openings located at positions corresponding to each of said penetration holes, so as to expose a part of said conductive layer for terminal pads at the bottom of each of said openings;

filling said penetration holes and said openings respectively with plating metals by electrolytic plating by using said conductive layer for terminal pads as an electric supply layer so that said plating metals form a metal column in each of said openings;

removing said plating resist so as to expose parts of said conductive layer for terminal pads other than a part where said metal column is formed;

removing said exposed parts of said conductive layer for terminal pads other than said part where said metal column is formed by etching so as to expose a surface of said insulating base, leaving said part where said metal column is formed as a terminal pad;

forming an insulating layer on said exposed surface of said insulating base, leaving an upper surface of said metal column uncovered; and

removing a part of said insulating layer near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column.

10. The interconnection substrate manufacturing method as claimed in claim 9,

wherein said conductive layer for terminal pads is composed of a metal containing copper, and said metal column is composed of solder, and

wherein the step of removing said exposed parts of said conductive layer for terminal pads is performed using an etching solution, an etching rate of said etching solution with respect to copper being higher than an etching rate of said etching solution with respect to solder.

11. A semiconductor device comprising:

a multilayer interconnection substrate which comprises an uppermost interconnection layer having a plurality of terminal pads formed at positions corresponding to a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said multilayer interconnection substrate; a metal column formed on each of said terminal pads; a resin film covering a side surface of said metal column; and an insulating layer formed on said uppermost interconnection layer so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film; and

a semiconductor element mounted on said multilayer interconnection substrate.

12. A semiconductor device comprising:

an interconnection substrate which

comprises an insulating base having a plurality of penetration holes; a plating metal filling each of said penetration holes; a terminal pad formed on an end of each of said penetration holes so that said terminal pad is connected to said plating metal, said terminal pad located at a position corresponding to a respective one of a plurality of external connection terminals provided on a semiconductor element which is to be mounted on said interconnection substrate; a metal column formed on said terminal pad; a resin film covering a side surface of said metal column; and an insulating layer formed on a surface of said insulating base on the same side as said end of each of said penetration holes so that a gap is formed between the insulating layer and an outer peripheral surface of said resin film; and

a semiconductor element mounted on said interconnection substrate.

13. A semiconductor device comprising:

a multilayer interconnection substrate manufactured by forming a plurality of terminal pads in an uppermost interconnection layer; forming an insulating layer on said uppermost interconnection layer; forming openings in said insulating layer, the openings located at positions corresponding to said terminal pads; filling each of said openings with metal particles; forming a metal column in each of said openings by heating said metal particles at a temperature which melts said metal particles; and removing a part of said insulating layer near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating

layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column; and

a semiconductor element mounted on said multilayer interconnection substrate.

14. A semiconductor device comprising:

an interconnection substrate manufactured by forming an insulating base having a plurality of penetration holes therein and a conductive layer for terminal pads formed on one surface thereof; forming a plating resist on said conductive layer for terminal pads; forming openings in said plating resist, the openings located at positions corresponding to each of said penetration holes, so as to expose a part of said conductive layer for terminal pads at the bottom of each of said openings; filling said penetration holes and said openings respectively with plating metals by electrolytic plating by using said conductive layer for terminal pads as an electric supply layer so that said plating metals form a metal column in each of said openings; removing said plating resist so as to expose parts of said conductive layer for terminal pads other than a part where said metal column is formed; removing said exposed parts of said conductive layer for terminal pads other than said part where said metal column is formed by etching so as to expose a surface of said insulating base, leaving said part where said metal column is formed as a terminal pad; forming an insulating layer on said exposed surface of said insulating base, leaving an upper surface of said metal column

uncovered; and removing a part of said insulating layer near but not adjacent to a peripheral side of said metal column, while leaving a part of said insulating layer adjacent to said peripheral side of said metal column, so that a gap is formed around but not adjacent to said peripheral side of said metal column; and

a semiconductor element mounted on said interconnection substrate.